WHAT IS CLAIMED IS:

1. A semiconductor device loading apparatus for test handlers, comprising:

a body including a plurality of pickup cylinders provided with a plurality of vacuum adsorbers for vacuum-sucking semiconductor and transferring devices to be tested, a space adjusting plate for adjusting pitches of the vacuum adsorbers, and an elevation guiding means for guiding lifting and lowering of the space adjusting plate; and

a guide block fixing plate formed to be separate from the body for guiding the semiconductor devices to be accurately positioned in pockets of a test tray, respectively.

2. The semiconductor device loading apparatus according to claim 1, wherein said space adjusting plate is provided with a plurality of guide slots formed to allow spaces therebetween to be downwardly narrowed so as to adjust pitches of the vacuum adsorbers, and said vacuum adsorbers are each provided with a guide projection adapted to be inserted to one of the guide slots.

3. The semiconductor device loading apparatus according to claim 1, wherein said guide block fixing plate is positioned to be downwardly spaced apart from the vacuum adsorbers and upwardly spaced apart from the test tray, and is provided with guide blocks of a number equal to the number of the pockets of the test tray.

4. The semiconductor device loading apparatus according to claim 3, wherein said guide blocks are each provided with an opening sized to be equal to a size of each of the semiconductor devices, and with a pair of guide pins downwardly extended

from front and rear edges thereof.

5. The semiconductor device loading apparatus according to claim 4, wherein said guide pins each have a diameter smaller than a diameter of each of the pin holes formed in front and rear edges of the pocket, and are spaced apart from each other by a space equal to a space between the pair of pin holes.

6. The semiconductor device loading apparatus according to claim 3, wherein said openings each comprise an entrance portion formed on an upper surface of the guide block and sized to be slightly larger than a size of each of the semiconductor devices to easily receive the semiconductor device, an exit portion formed on a lower surface of the guide block and sized to be substantially equal to a size of the semiconductor device to allow the semiconductor device to pass therethrough, and a guide portion formed between the entrance and exit portions and tapered from the entrance portion to the exit portion.